a time slice instruction counter that counts a number of instructions executed with respect to a given background task; and

a background task controller that cyclicly activates a context corresponding to another background task when said number equals a dynamically-programmable time slice value.

(2) Kindly amend Claim 8 as follows:

8. (Amended) A method of managing multitasking of a plurality of tasks including foreground tasks and background tasks in a processor, comprising the steps of:

counting a number of instructions executed with respect to a given background task; and

cyclicly activating a context corresponding to another background task when said number equals a dynamically-programmable time slice value.

(3) Kindly amend Claim 15 as follows:

15. (Amended) A processor, comprising:

an instruction decoder that decodes instructions received into said processor and corresponding to a plurality of tasks which includes foreground tasks and background tasks;

a plurality of register sets, corresponding to said plurality of tasks, that contain operands to be manipulated;

an execution core, coupled to said instruction decoder and said plurality of register sets, that executes instructions corresponding to an active one of said plurality of tasks to manipulate ones of said operands; and

a context controller, coupled to said instruction decoder and said execution core, that manages multitasking with respect to said plurality of tasks, including:

a time slice instruction counter that counts a number of instructions executed with respect to a given background task; and

a background task controller that cyclicly activates a context corresponding to another background task when said number equals a dynamically-programmable time slice value.